REMARKS

35 U.S.C. Section 102 Rejections

The above referenced Office Action states that independent Claims1, 7, and 13 are rejected as being anticipated by Ma (US Patent No. 6320437) and Stark (U.S. P.A.P. 20020017936 A1). Applicant has amended independent Claims 1, 7, 13, and 19 to more particularly point out aspects of the present invention. Applicant respectfully asserts that the claimed embodiments as recited in the newly amended independent Claims 1, 7, and 13 are not anticipated by the Ma reference.

Applicants have herein amended independent Claims 1, 7, 13, and 19 to particularly point out that two inputs comprising two separate signals are used to control the latch circuit, as recited in Claims 1 and 7, or alternatively, the timing generator circuit, as recited in Claims 13 and 19. These limitations are not shown by the cited references.

The Ma reference discloses a duty cycle regulator circuit that derives an output clock signal having an adjustable duty cycle from a single input clock signal. The cited "clock pulse generator 30" of Figure 2 of Ma receives the input clock signal "CLK_IN 33" and generates therefrom a set signal for the "clock output unit 10." The signal at node 34 is used by the clock output means 10 to generate CLK_OUT and CLK_OUT-which is subsequently received by the clock pulse generator 30 to create the signals for the clock output unit 10. The reset signal is generated from

the output of the clock pulse generator 30. The reset signal for the clock output unit 10 is described as a pulse provided by buffers of a delay circuit. As such, the reset signal does not comprise a second input, but is merely a delayed version of the output of the clock output unit 10.

The Ma reference has no discussion or disclosure in the description of figure 2 for the use of the CLK_IN signal at node 33 to produce the reset output at node 23. The Ma reference explicitly describes the use of the output clock signal fed back to input port 21 of the delay unit 22 produce the reset pulse at output port 23. Importantly, Applicants find no discussion or disclosure of the use of the clock in signal 33 by the delay unit 20.

In contrast, independent Claims 1 and 7 have been amended to recite the use of two separate input signals. The rising edge of the internal clock signal is triggered at a rising edge of the external clock signal by the edge detection circuit. Independent Claims 13 and 19 have been amended to recite two separate input signals, wherein the rising edge of the external clock signal sets the timing generator circuit to produce a rising edge of the internal clock signal and the VCRO signal resets the timing generator circuit to produce a falling edge of the internal clock signal.

This is completely different from Ma, where the reset signal is explicitly disclosed as being generated from the output of the "clock output unit 10" of Ma. Thus, Applicant respectfully asserts that the present invention as recited in the amended independent Claims 1, 7, 13, and 19 is not anticipated by the Ma reference within the meaning of 35 U.S.C. Section 102.

With respect to Independent claim 13, claim 13 has been amended to recite two separate input signals, wherein the rising edge of the external clock signal setting the timing generator circuit to produce a rising edge of the internal clock signal and the VCRO signal resets the timing generator circuit to produce a falling edge of the internal clock signal. These limitations are not shown by Stark or Ma.

35 U.S.C. Section 103 Rejections

Independent claim 19 is rejected under 35 U.S.C. § 103 as being rendered unpatentable by Ma in view of Huynh (U.S. Publication No. 2003/0107432) and Stark in view of Huynh. Applicant has amended independent Claims 1, 7, 13, and 19 to more particularly point out aspects of the present invention. Applicant respectfully asserts that the present invention as recited in newly amended independent Claims 1, 7, 13, and 19 is not rendered unpatentable by Ma and Huynh within the meaning of 35 U.S.C. § 103.

The addition of the Huynh reference does not cure the shortcomings of Stark or Ma. Huynh is relied upon to show a switched capacitor component of an ADC (Analog to Digital Converter). The cited combination does not show or suggest a latch circuit using two inputs, one from the edge detect circuit that yields the rising edge of the internal clock signal and one from the conditioned signal that yields the falling edge of the internal clock signal. The cited combination does not show or suggest a VCRO input used in conjunction with the edge detect circuit (e.g., as in independent Claims 13 and 19). The cited combination does not show or suggest the rising edge of the external clock signal setting the timing generator circuit to produce a rising edge of the internal clock signal and the VCRO signal resets the timing generator circuit to produce a falling edge of the internal clock signal. Accordingly, the cited combination does not render the present invention obvious as recited in independent Claims 1, 7, 13, and 19 within the meaning of 35 U.S.C. Section 103.

CONCLUSION

For the reasons discussed above, Applicant respectfully asserts that the 35 U.S.C. § 102 rejections and 35 U.S.C. § 103 rejections are overcome. Applicant respectfully submits that all remaining claims (Claims 1-3, 5-9, 11-15, 17-21, and 23) of the present application are now allowable.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,
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